FAIRCHILD SEMICONDUCTOR™

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DM74LS112A

Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flop with Preset, Clear, and Complementary Outputs

General Description

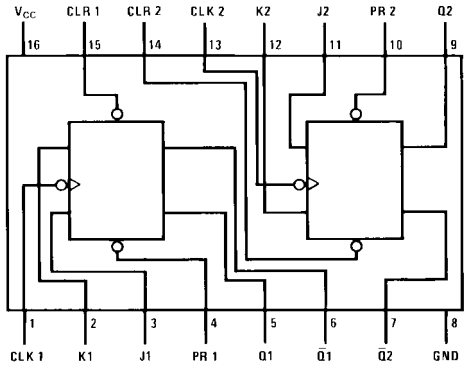
This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the falling edge of the clock pulse. Data on the J and K inputs may be changed while the clock is HIGH or LOW without affecting the outputs as long as the setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Ordering Code:

Order Number	Package Number	Package Description
DM74KS112AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS112AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level
↓ = Negative Going Edge of Pulse
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Note 1: This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (HIGH) level.

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Absolute Maximum Ratings(Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 3)		0		30	MHz
f_{CLK}	Clock Frequency (Note 5)		0		25	MHz
t_W	Pulse Width (Note 3)	Clock HIGH	20			ns
		Preset LOW	25			
		Clear LOW	25			
t_W	Pulse Width (Note 5)	Clock HIGH	25			ns
		Preset LOW	30			
		Clear LOW	30			
t_{SU}	Setup Time (Note 3)(Note 4)		20↓			ns
t_{SU}	Setup Time (Note 4)(Note 5)		25↓			ns
t_H	Hold Time (Note 3)(Note 4)		0↓			ns
t_H	Hold Time (Note 4)(Note 5)		5↓			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 3: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 4: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 5: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –18 mA				–1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Preset			0.3	
			Clock			0.4	
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	µA
			Clear			60	
			Preset			60	
			Clock			80	
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			–0.4	mA
			Clear			–0.8	
			Preset			–0.8	
			Clock			–0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 7)		–20		–100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 8)			4	6	mA

Note 6: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.125V with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

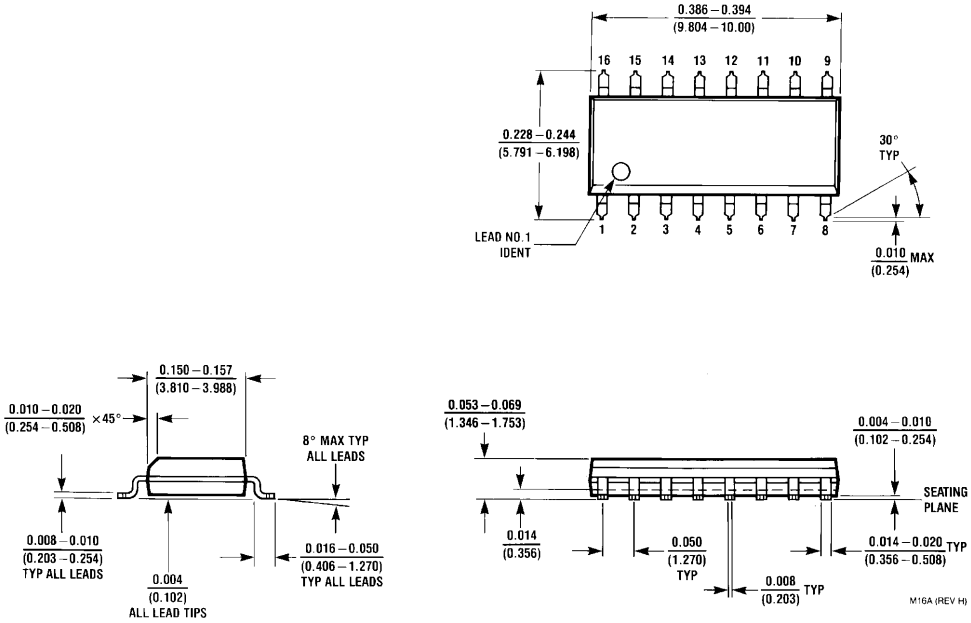
Note 8: With all outputs OPEN, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn. At the time of measurement the clock is grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

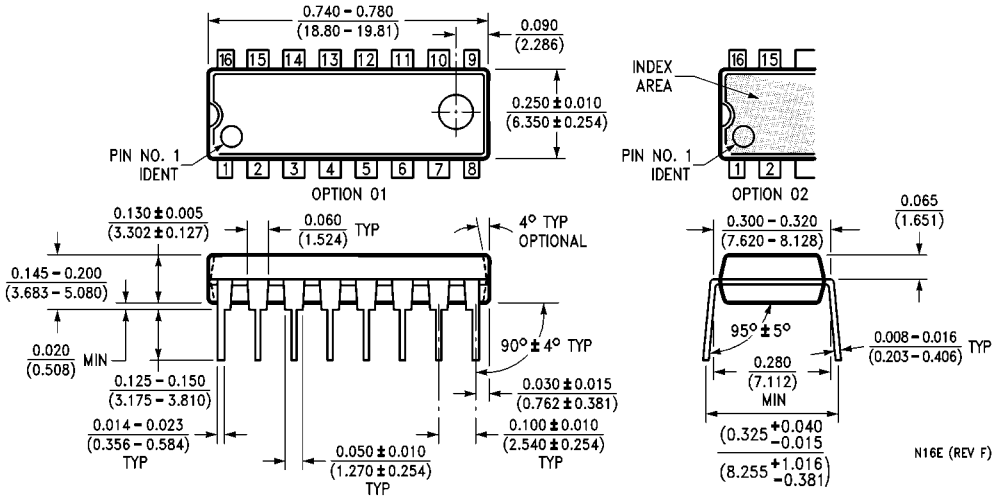
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		20		24	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\overline{Q}$		20		28	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		20		28	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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